AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1-7. (Canceled).

8. (Previously Presented) A processor, comprising:

a clock signal generator generating clock signals;

an operational processing part performing data processing which is divided into a plurality of execution units, in accordance with the clock signals;

a storage storing data per each execution unit, the execution unit being executed by the operational processing part as a unit;

a data amount detector detecting amounts of the data stored in the storage per each execution unit;

a clock frequency determining part determining a new clock frequency of the clock signals by using the amounts of the data, said clock signals being supplied newly to the operational processing part,

the clock frequency determining part including a table indicating the relation between the amounts of the data detected by the data amount detector and the variation of the clock frequency, a clock frequency holder holding a practical current clock frequency supplied to the operational processing part, and an adder adding to the current clock frequency the variation

obtained from the table, the clock frequency determining part determining newly the output value of the adder as the clock frequency of the clock signals;

an execution status detector detecting whether a certain execution unit becomes the predetermined state or not;

a timer newly starting the clocking when the execution status detector detects that the execution unit has become the predetermined state; and

a clock frequency changing part changing the clock frequency, the clock frequency changing part decreasing the absolute value of the variation according to the value of the timer,

wherein the adder adds to the current clock frequency the variation which is changed by the clock frequency changing part.

9-15. (Canceled).

16. (Currently Amended) A clock frequency determining method determining a clock frequency supplied to a processor, which comprises: an operational processing part processing data in accordance with clock signals; a storage storing the data per an execution unit, the execution unit being executed by the operational processing part as a unit; a data amount detector detecting amounts of the data stored in the storage per each execution [[unti]] unit; a clock frequency determining part determining the clock frequency and having a table indicating the relation between the amounts of the data detected by the data amount detector and the variation of the clock frequency; an

execution status detector detecting a status of a certain execution unit; a timer timing the detection of the execution status detector; a clock frequency changing part changing the variation of the clock frequency, the method comprising:

detecting amounts of data associated with the respective execution units, said data being stored in the storage;

detecting whether a certain execution unit becomes a predetermined state or not, by using the execution status detector;

starting the timing when the execution status detector detects that the execution unit has become the predetermined state by using the timer;

changing the clock frequency, so that the absolute value of the variation is decreased according to the value of the timer by using the clock frequency changing part;

adding the variation of the clock frequency to the current clock frequency, the variation of the clock frequency being obtained from the table and being changed by the clock frequency changing part;

determining a result of the addition as a new clock frequency to be supplied to the operational processing part; and

generating clock signals supplied to the operational processing part in accordance with the new clock frequency.